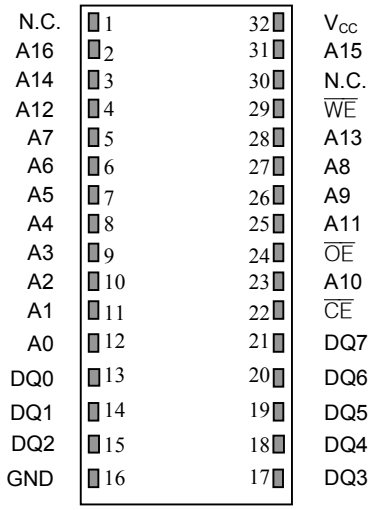
DS1646/DS1646P
Nonvolatile Timekeeping RAM

FEATURES

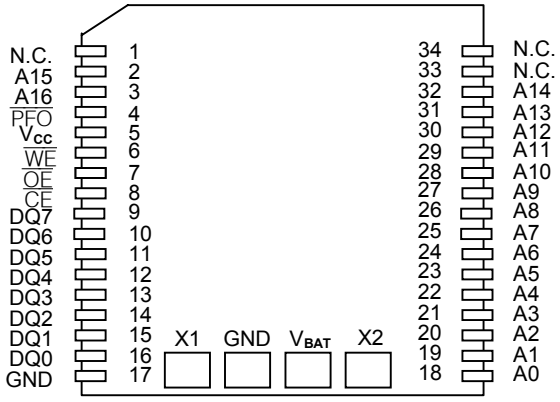
- Integrates NV SRAM, Real-Time Clock, Crystal, Power-Fail Control Circuit and Lithium Energy Source
- Clock Registers are Accessed Identically to the Static RAM. These Registers are Resident in the Eight Top RAM Locations
- Totally Nonvolatile with Over 10 Years of Operation in the Absence of Power
- BCD-Coded Year, Month, Date, Day, Hours, Minutes, and Seconds with Leap Year Compensation Valid Up to 2100
- Power-Fail Write Protection Allows for ±10% V_{CC} Power Supply Tolerance
- DS1646 only (DIP Module)
  - Standard JEDEC Bytewide 128k x 8 RAM Pinout
- DS1646P Only (PowerCap® Module Board)
  - Surface Mountable Package for Direct Connection to PowerCap Containing Battery and Crystal
  - Replaceable Battery (PowerCap)
  - Power-Fail Output
  - Pin-for-Pin Compatible with Other Densities of DS164xP Timekeeping RAM
  - Underwriters Laboratory (UL) Recognized

PowerCap is a registered trademark of Dallas Semiconductor.

PIN CONFIGURATIONS



32-Pin Encapsulated Package



34-Pin PowerCap Module Board
(Uses DS9034PCX PowerCap)

ORDERING INFORMATION

PART	VOLTAGE RANGE (V)	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS16460-120	5.0	0°C to +70°C	32 EDIP (0.740a)	DS1646+120
DS16460-120	5.0	0°C to +70°C	32 EDIP (0.740a)	DS1646-120
DS1646P-120	5.0	0°C to +70°C	34 PowerCap*	DS1646P+120
DS1646P-120	5.0	0°C to +70°C	34 PowerCap*	DS1646P-120

**DS9034-PCX, DS9034I-PCX, DS9034-PCX+ required (must be ordered separately).*

A "+" indicates a lead-free product. The top mark will include a "+" symbol on lead-free devices.

DESCRIPTION

The DS1646 is a 128k x 8 nonvolatile static RAM with a full-function real time clock, which are both accessible in a byte-wide format. The nonvolatile timekeeping RAM is functionally equivalent to any JEDEC standard 128k x 8 SRAM. The device can also be easily substituted for ROM, EPROM and EEPROM, providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double-buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1646 also contains its own power-fail circuitry, which deselects the device when the V_{CC} supply is in an out-of-tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

PACKAGES

The DS1646 is available in two packages: 32-pin DIP and 34-pin PowerCap module. The 32-pin DIP style module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap Module Board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the DS1646P after the completion of the surface mount process. Mounting the PowerCap after the surface mount process prevents damage to the crystal and battery due to the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap Module Board and PowerCap are ordered separately and shipped in separate containers. The part number for the PowerCap is DS9034PCX.

CLOCK OPERATIONS—READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1646 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the 7th most significant bit in the control register. As long as 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was present at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that clock accuracy is not affected by the access of data. All of the DS1646 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to 0.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +7.0V
Storage Temperature Range……-40°C to +85°C, Noncondensing
Soldering Temperature……260°C for 10 seconds (DIP Package) (See Note 7)
See IPC/JEDEC Standard J-STD-020 for Surface-Mount Devices

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C, Noncondensing	5V ±10%

RECOMMENDED DC OPERATING CONDITIONS (Over the Operating Range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Voltage All Inputs	V_{IH}	2.2		V_{CC}+0.3	V	
Logic 0 Voltage All Inputs	V_{IL}	-0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS (Over the Operating Range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}			85	mA	2, 3
TTL Standby Current ($\overline{CE}$ =V_{IH})	I_{CC2}		3	6	mA	2, 3
CMOS Standby Current ($\overline{CE}$ =V_{CC}-0.2V)	I_{CC3}		2	4.0	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4	V	
Power-Fail Voltage	V_{PF}	4.0	4.25	4.5	V	

AC ELECTRICAL CHARACTERISTICS (Over the Operating Range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
Address Access Time	t_{AA}			120	ns	
$\overline{CE}$ Access Time	t_{CEA}			120	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}			40	ns	
Output Enable Access Time	t_{OEA}			100	ns	
Output Enable Data Off Time	t_{OEZ}			40	ns	
Output Enable to DQ Low-Z	t_{OEL}	5			ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5			ns	
Output Hold from Address	t_{OH}	5			ns	
Write Cycle Time	t_{WC}	120			ns	
Address Setup Time	t_{AS}	0			ns	
$\overline{CE}$ Pulse Width	t_{CEW}	100			ns	
Address Hold from End of Write	t_{AH1}	5			ns	5
	t_{AH2}	30			ns	6
Write Pulse Width	t_{WEW}	75			ns	
$\overline{WE}$ Data Off Time	t_{WEZ}			40	ns	
$\overline{WE}$ or $\overline{CE}$ Inactive Time	t_{WR}	10			ns	
Data Setup Time	t_{DS}	85			ns	
Data Hold Time High	t_{DH1}	0			ns	5
	t_{DH2}	25			ns	6

AC TEST CONDITIONS

Input Levels: 0V to 3V
Transition Times: 5 ns

CAPACITANCE (T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on All Pins (except DQ)	C_I			7	pF	
Capacitance on DQ Pins	C_{DQ}			10	pF	

AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (Over the Operating Range)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{PF} (Max) to V_{PF} (Min) V_{CC} Fall Time	t_F	300			µs	
V_{PF} (Min) to V_{SO} V_{CC} Fall Time	t_{FB}	10			µs	
V_{SO} to V_{PF} (Min) V_{CC} Rise Time	t_{RB}	1			µs	
V_{PF} (Min) to V_{PF} (Max) V_{CC} Rise Time	t_R	0			µs	
Power-Up	t_{REC}	15		35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	4

NOTES:

1) All voltages are referenced to ground.
2) Typical values are at 25°C and nominal supplies.
3) Outputs are open.
4) Data retention time is at 25°C and is calculated from the date code on the device package. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225 would mean the 25th week of 1992.
5) t_{AH1}, t_{DH1} are measured from $\overline{WE}$ going high.
6) t_{AH2}, t_{DH2} are measured from $\overline{CE}$ going high.
7) Real-Time Clock Modules (DIP) can be successfully processed through conventional wave-soldering techniques as long as temperatures as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used.

   In addition, for the PowerCap version:
   a. Dallas Semiconductor recommends that PowerCap Module bases experience one pass through solder reflow oriented with the label side up (“live-bug”).
   b. Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflows and use a solder wick to remove solder.